EE 434
Lecture 9

Process Technology

- Contacts, Interconnects, Metalization
- Interconnect Components
  - Resistors
  - Capacitors

Review from Last Time

- Diffusion is used to force migration of impurity atoms into substrate
  - Time and temperature dependent
  - Type of grading can be controlled
  - Subject to subsequent movement when other warm processing steps are done
- Epitaxy
  - Single crystalline extension of substrate
  - Grows slowly to maintain crystalline structure
- Polysilicon
- Used for gates of transistors
  - Comprised of many small crystals
  - Makes good conductor if heavily doped
  - Makes good resistor if moderately doped

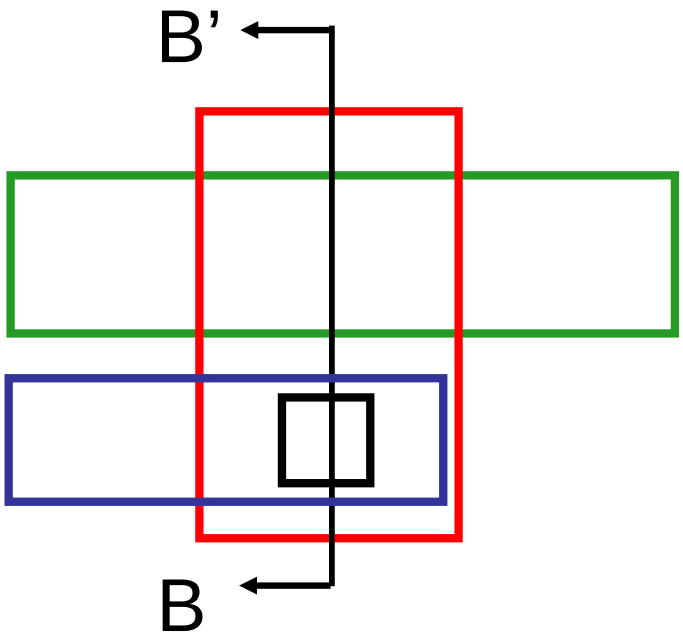
IC Fabrication Technology

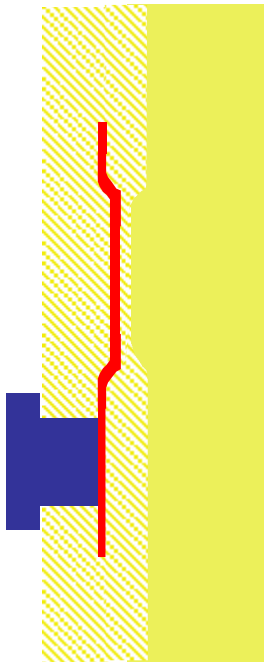
- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization

Contacts, Interconnect and Metalization

- Contacts usually of a fixed size
  - All etches reach bottom at about the same time
  - Multiple contacts widely used
  - Contacts not allowed to Poly on thin oxide in most processes
  - Dog-bone often needed for minimum-length devices

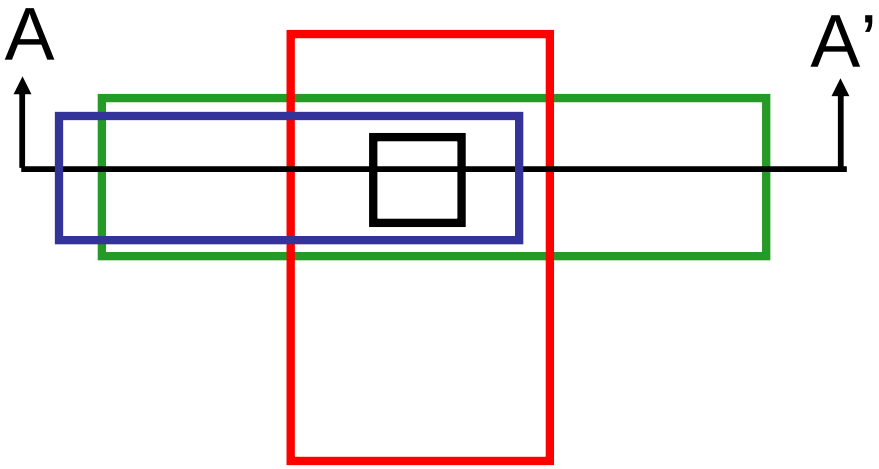
Contacts

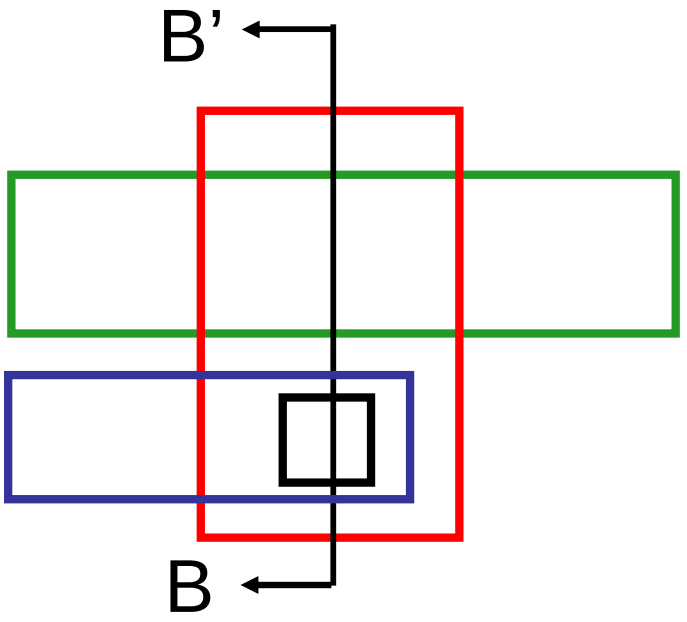




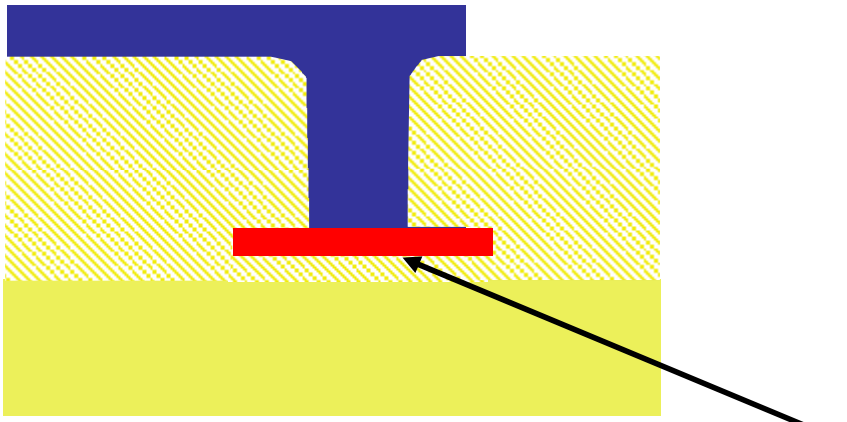
Acceptable Contact

Contacts





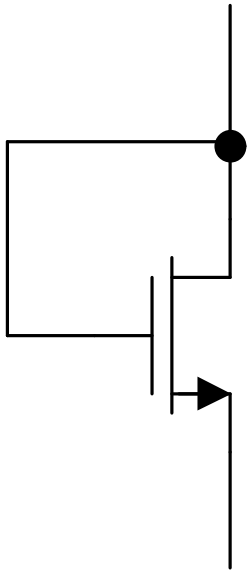
Acceptable Contact



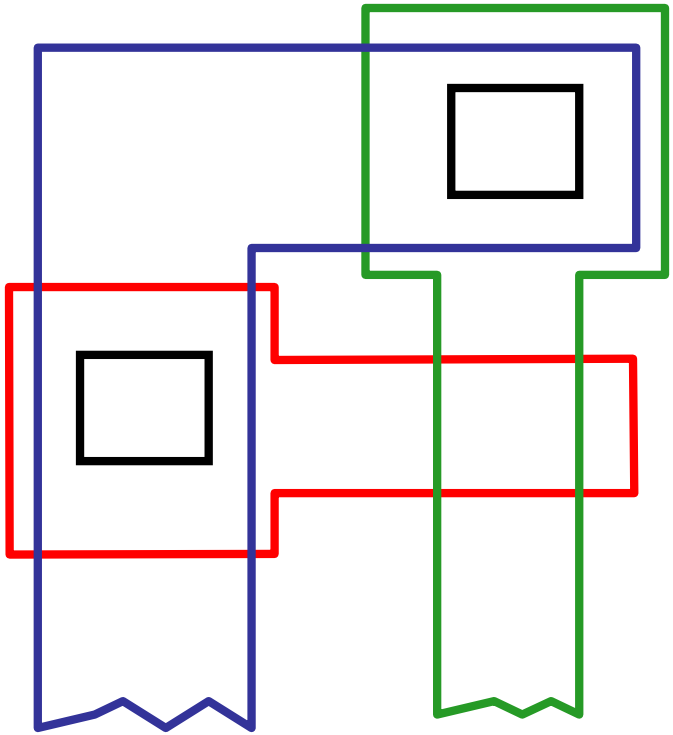
Vulnerable to pin holes

Unacceptable Contact

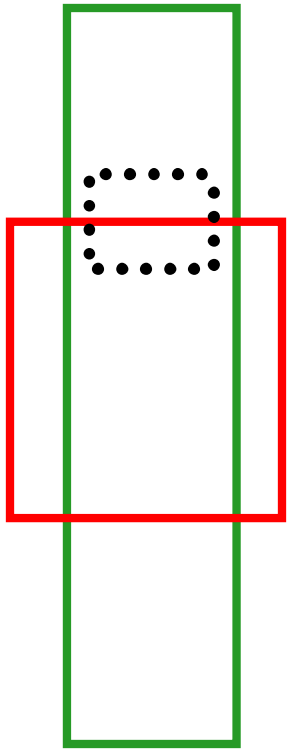
Contacts



Common
Circuit
Connection



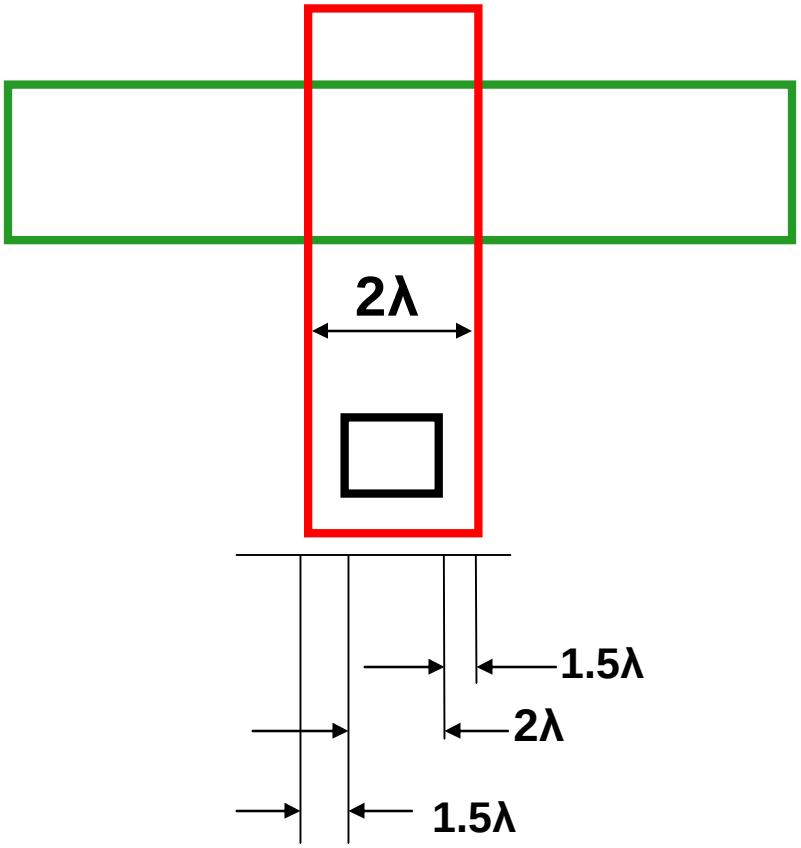
Standard Interconnection



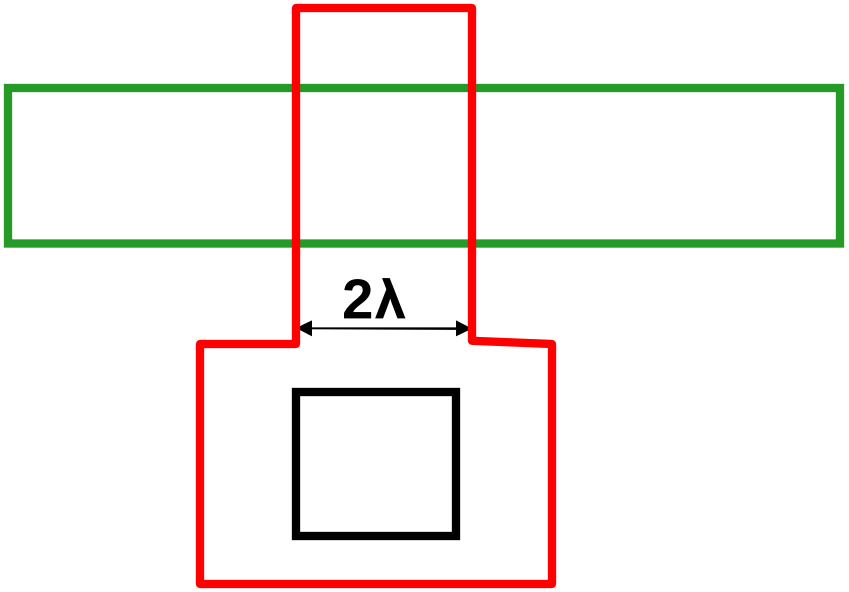
Buried Contact

Can save area but not
allowed in many processes

Contacts



Design Rule Violation

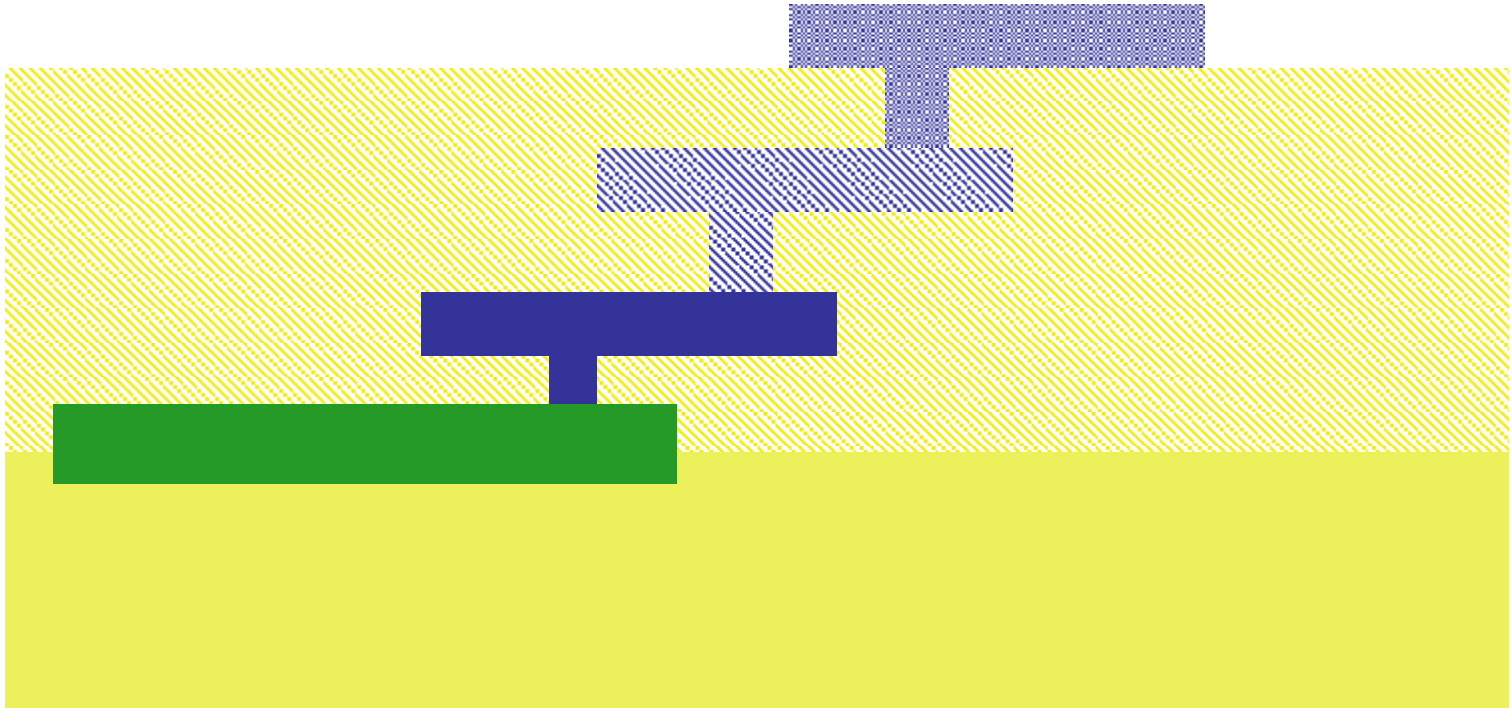


“Dog Bone” Contact

Metalization

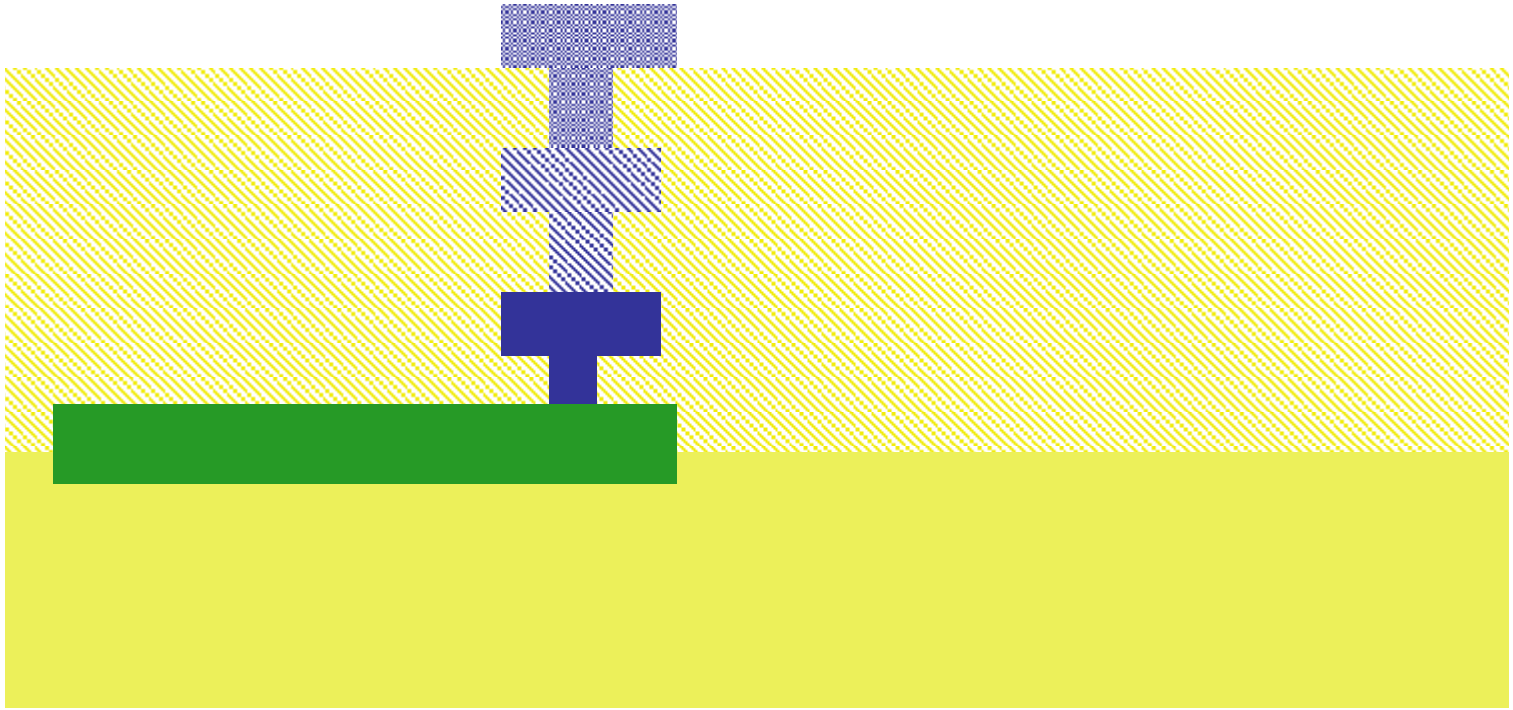
- Aluminum widely used for interconnect
- Copper finding some applications
- Must not exceed maximum current density
  - around 1ma/u
- Ohmic Drop must be managed
- Parasitic Capacitances must be managed
- Interconnects from high to low level metals require connections to each level of metal
- Stacked vias permissible in some processes

Multiple Level Interconnects



3-rd level metal connection to n-active without stacked vias

Multiple Level Interconnects

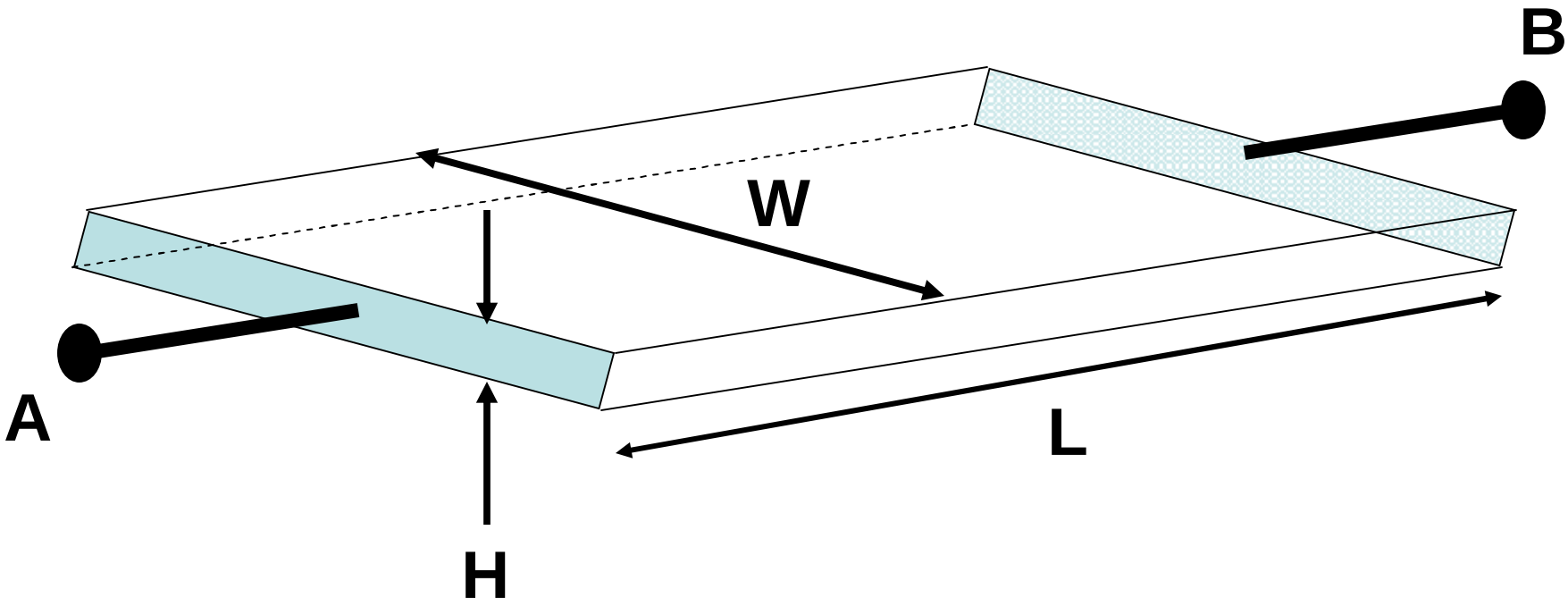


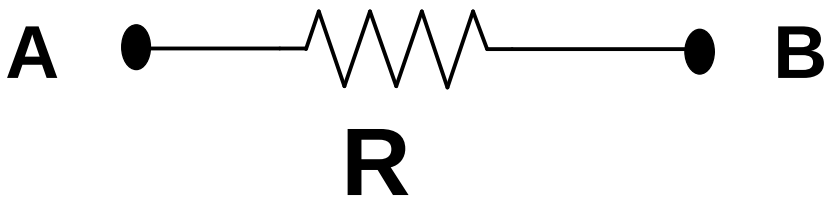
3-rd level metal connection to n-active with stacked vias

Interconnects

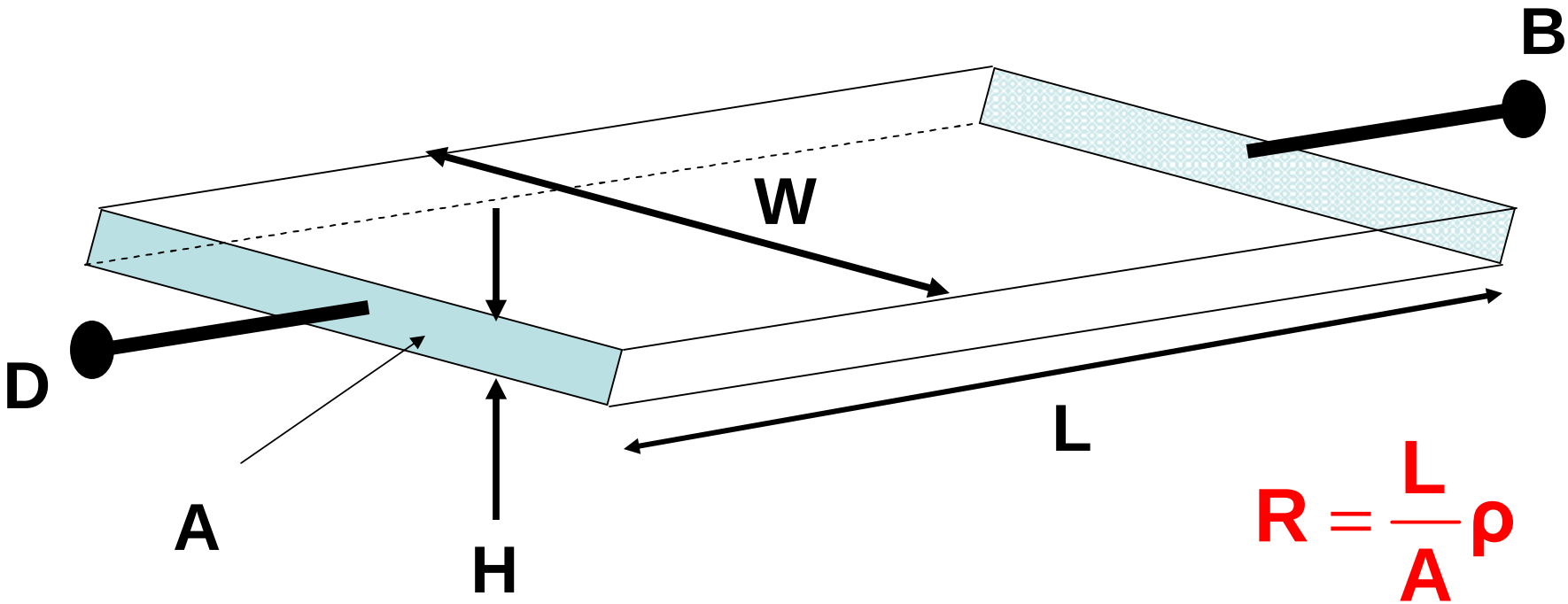
- Metal is preferred interconnect
  - Because conductivity is high
- Parasitic capacitances and resistances of concern in all interconnects
- Polysilicon used for short interconnects
  - Silicided to reduce resistance
  - Unsilicided when used as resistors
- Diffusion used for short interconnects
  - Parasitic capacitances are high

Resistance in Interconnects

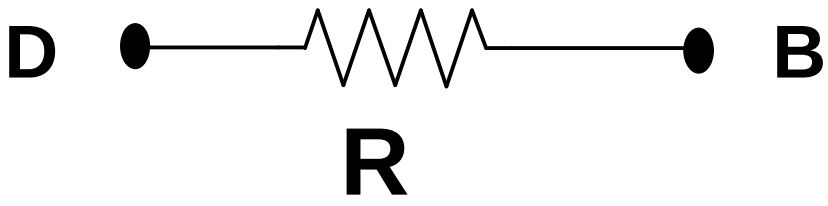




Resistance in Interconnects



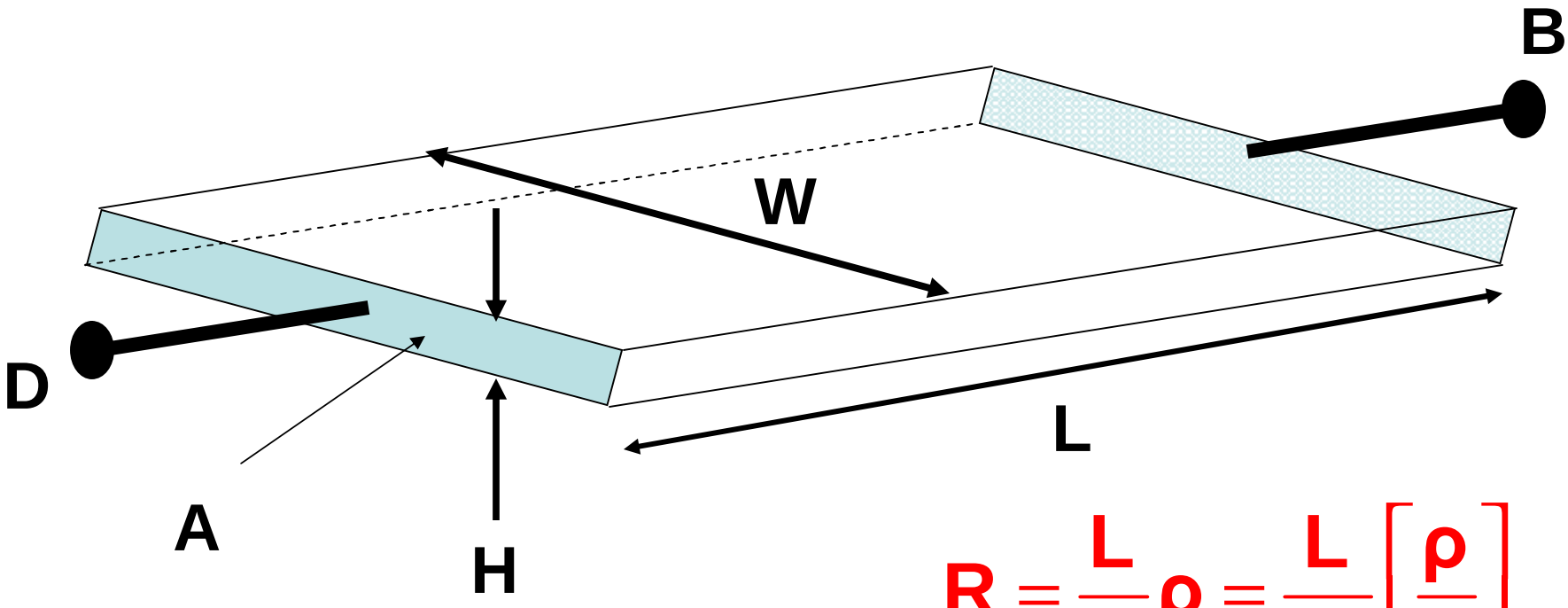
$$R = \frac{L}{A}\rho$$



A=HW

ρ independent of geometry and characteristic of the process

Resistance in Interconnects



$$R = \frac{L}{A}\rho = \frac{L}{W}\left[\frac{\rho}{H}\right]$$

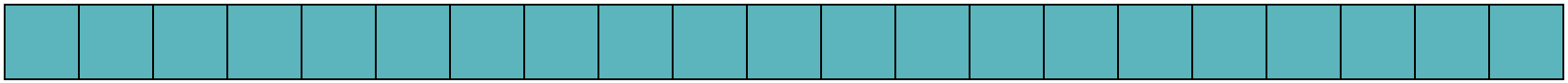
H << W and H << L in most processes
Interconnect behaves as a “thin” film
Sheet resistance often used instead of conductivity to characterize film

$R_{\square}=\rho/H$ $R=R_{\square}[L / W]$

Resistance in Interconnects

$$R = R_{\square}[L / W]$$

The “Number of Squares” approach to resistance determination in thin films

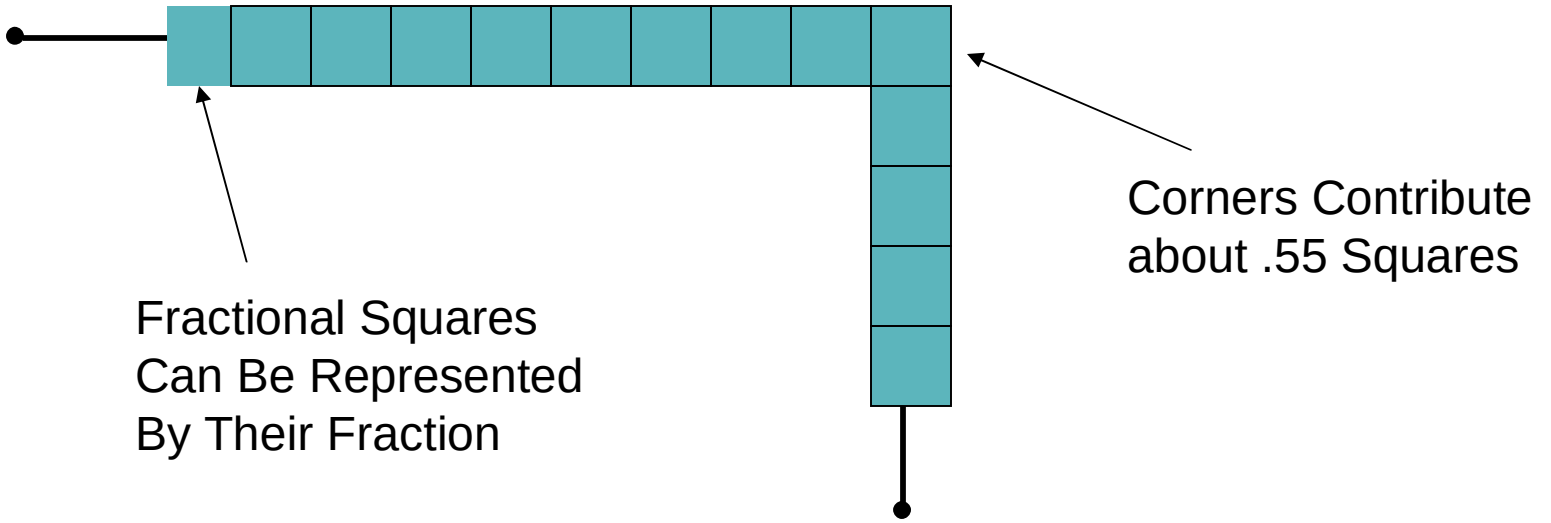


$N_S = 21$

$L / W = 21$

$$R = R_{\square} N_S$$

Resistance in Interconnects



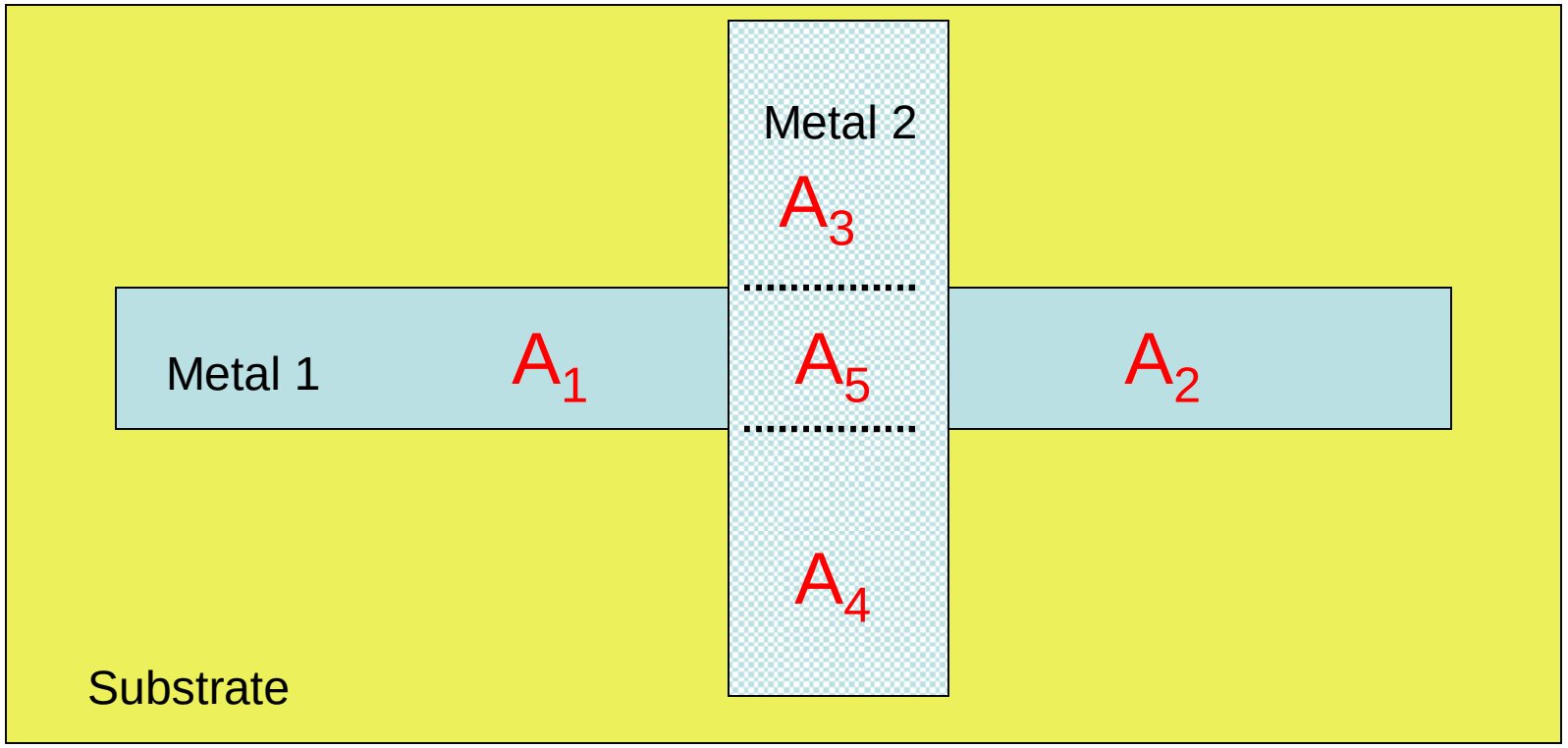
The “squares” approach is not exact but is good enough for calculating resistance in almost all applications

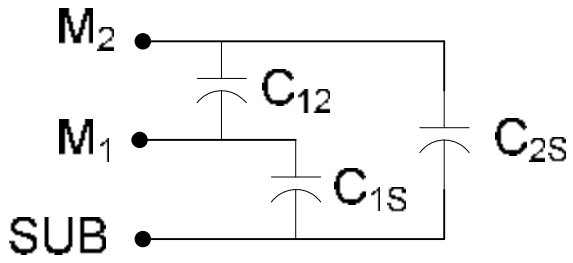
In this example:

$$N_S = 12 + .55 + .7 = 13.25$$

$$\mathbf{R = R_{\square} 13.25}$$

Capacitance in Interconnects





Equivalent Circuit

$C_{12}=CD_{12}\,A_5$

$C_{1S}=CD_{1S}\,(A_1+A_2+A_5)$

$C_{2S}=CD_{2S}\,(A_3+A_4)$

End of Lecture 9